OCTAVE BANDWIDTH HIGH SPEED LIMITER WITH UNIFORM SUPPRESSION CHARACTERISTICS

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Abstract

The performance of several octave-bandwidth diode clipper/limiters having uniform suppression characteristics over the 2.0 to 4.0 GHz octave is discussed. Suppression over the band is 4.0 dB or greater for a structure using Silicon diodes and 3.5 dB or greater for a similar structure using GaAs diodes.

The design of a low power, high speed, octave bandwidth clipper/limiter is complicated if in addition to the large signal (P_L) to be compressed ($C_L = P_{Li}/P_{Lo}$), other small signals (P_s) are present and must be compressed ($C_s = P_{si}/P_{so}$) even more, i.e. $C_s > C_L$. Define suppression (S) = C_s/C_L. It is apparent that a high speed diode must be used as the clipper, but unfortunately such a diode is also an efficient generator of harmonics of the large signal (mf_L) and mixing products of the simultaneously present large and small signals ($mf_L \pm nf_s$).

It has been shown that an anti-parallel diode pair[1] having input frequencies of f_L and f_s can only generate outputs $mf_L \pm nf_s$ when m + n is an odd integer. If the two diodes of the anti-parallel pair were identical then all odd harmonics and mixing products for which m + n is an even integer would be constrained to flow only within the loop formed by the pair of diodes. Finite unbalance between the two diodes will of course lessen the suppression of these odd integer outputs. The effect of diode unbalance in this structure has been analyzed[2]. Figure 1 illustrates the output spectrum of the limiter to be described when the input is a signal at 3 GHz at + 1 dBm. Fundamental mixing products ($f_L \pm f_s$) are suppressed as are half of the normally present higher order intermodulation products of which only $2f_L - f_s$ is both significant and in band.

For the ideal (hard) limiter, it can be shown that the maximum suppression is 6 dB[3,4] when there is one interfering signal. This may easily be seen by using the orthogonal nature of AM and FM (low index) to decompose the pair of signals into AM and FM characteristics. The elimination of the AM sidebands by the limiting action will therefore result in a pair of FM sidebands of equal amplitude (but out of phase by 180°), each of which is reduced from the original by 6 dB.

A sketch and photograph of the structure to be discussed are given in Figures 2 and 3, respectively. It consists of two anti-parallel diode pairs shunt-mounted across a 50 ohm transmission line and two capacitances whose values and exact locations relative to the diode locations are chosen to achieve the required broad-band performance. The present structure was designed to operate over the 2.0 to 4.0 GHz range on microstrip using a 0.025" thick alumina ($\epsilon_r = 9.6$) substrate. This particular choice of circuit is based on the requirement of operation over an octave band.

Tests were conducted on a single-pair version of the limiter using both Si and GaAs (Schottky) diodes of approximately equal junction diameters. A comparison of the two is given in Figure 4. Note that the onset of compression is different because of the different junction potentials. The maximum suppression for the silicon diode limiter is 2 dB, and for the GaAs diode limiter it is 3.5 dB. The input power level at which the onset of compression occurs can be varied through the use of dc bias but at the expense of a somewhat more complex circuit structure.

Measurements of compression and suppression were made on the double anti-parallel pair limiter which is schematically illustrated in Figure 2. Silicon diodes, manufactured by Microwave Associates, Burlington, Massachusetts, were used. The diodes were mounted across a .010 inch gap between a 50 ohm transmission line and a metallized pad which was grounded over the edge of the substrate. Compression and suppression characteristics for f_L = 3.00 GHz and f_s = 2.95 GHz are plotted in Figure 5. Similar curves were generated for f_L = 2.00 and 4.00 GHz. The maximum suppression in all three cases was 4 dB or greater. The input power range over which suppression was 3 dB or better was 9 dB in all cases.

The input return loss at a power level of + 1 dBm was greater than 10 dB over the 2.00 to 4.00 GHz band. The small signal insertion loss was 1.0 ± .5 dB and the small signal return loss was greater than 13 dB over the band.

Using a similar double anti-parallel pair structure, a limiter was constructed using GaAs Schottky barrier diodes manufactured by Westinghouse. The diodes have a junction diameter of 10 microns and a cutoff frequency in the range of 600 - 800 GHz. Tuning of the device was accomplished by placing lumped capacitances across the 50 ohm transmission line on both the input and output sides of the structure. The tuning criterion was to obtain minimum variation of suppression across the 2 GHz to 4 GHz band at an input large signal power level of + 11 dBm.

Measurements were made of the P_{out} vs P_{in} characteristic at 2.0, 3.0, and 4.0 GHz. Swept frequency measurements were then made of the small signal transmission through the device over the 2.0 to 4.0 GHz band with the large signal (at several levels) at each of the above three frequencies. The swept measurements therefore resulted in $C_s(f)$, as defined earlier, for each frequency and power level of the large signal. The suppression $[S(f) = C_s(f)/C_L]$ was then computed using the appropriate value of C_L, the large signal compression. Figure 6 illustrates the variations of suppression across the band for several large signal levels with f_L = 3.0 GHz. The drop in suppression at the high end of the band for large signal levels may be attributed to the de-tuning effect of the large average capacitance of the diodes under large drive conditions.

The variation of suppression with input power level at a fixed f_L = 3.0 GHz and f_s = 3.0 GHz is illustrated in Figure 7. The P_{out} vs P_{in} characteristic at that frequency is also shown.

Conclusions

The double anti-parallel diode pair limiter has been shown to have characteristics which may be beneficial in applications where broad band limiting and suppression are required. The particular structure discussed here makes use of two design criteria. First, it approaches the hard limiter ideal by presenting a higher input admittance at a given RF voltage than would be the case with a single diode or a single anti-parallel pair. Second, the spacing of the pairs is chosen to resonate the diode parasitic capacitance and thus increase the total RF voltage across the diodes. The tuning capacitors are used to broad band this resonance.

References

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2. M. Cohn, J. E. Degenford, and B. A. Newman, "Harmonic Mixing With An Anti-Parallel Diode Pair," to be published in IEEE Trans. on MTT, 1975.
3. Lyons, R. G., "The Effect of Hard Limiting on Signal to Interference Ratios," Research Report No. 69-1, Department of Mathematics, Queen's University, Kingston, Ontario, February 1969.
4. Jones, J. J., "Hard Limiting of Two Signals in Random Noise," IEEE Transactions on Information Theory, Vol. 9, pp 34, January 1963.

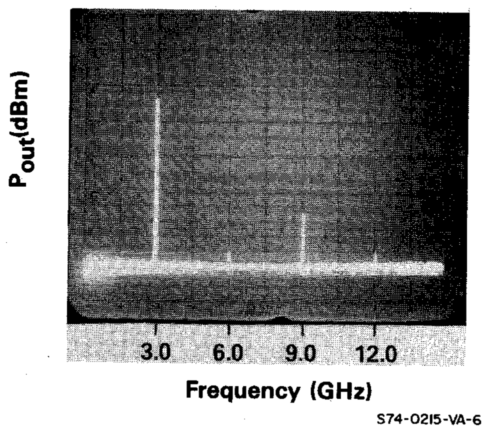


Figure 1 - Limiter output for an input signal of + 1 dBm at 3.0 GHz. Lines correspond to 3.0, 6.0, 9.0, and 12.0 GHz. Log ref = + 20 dBm, 10 dB/div.

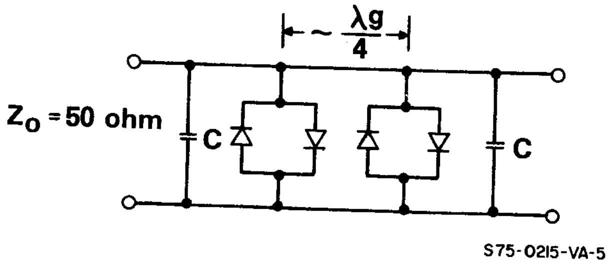


Figure 2 - Double anti - parallel pair limiter with capacitive tuning.

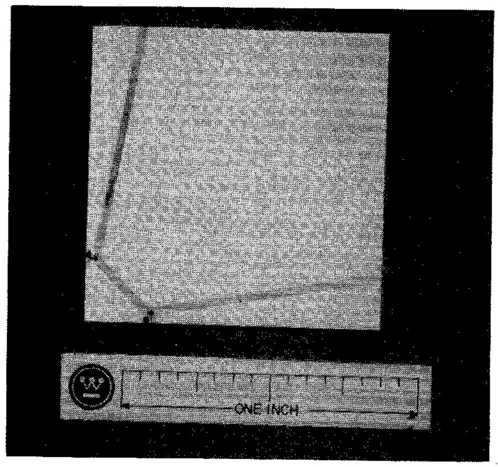


Figure 3 - Photograph of double anti - parallel pair limiter (tuning capacitances not shown).

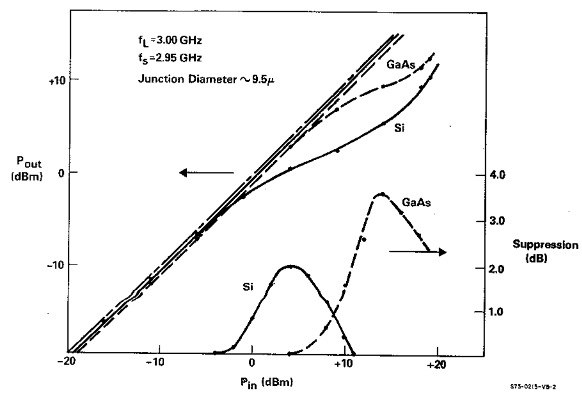
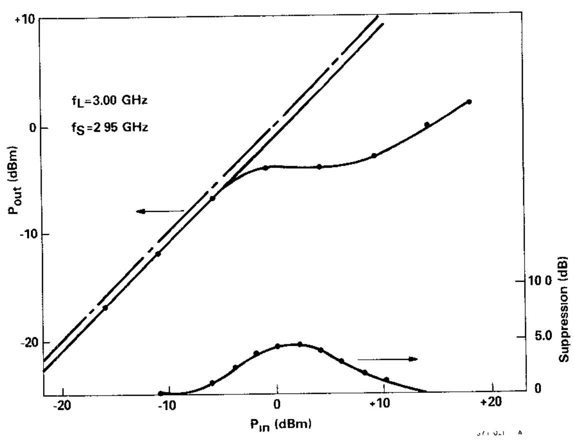


Figure 4 - Comparison of Si and GaAs diode single anti-parallel pair limiters at 3.0 GHz.



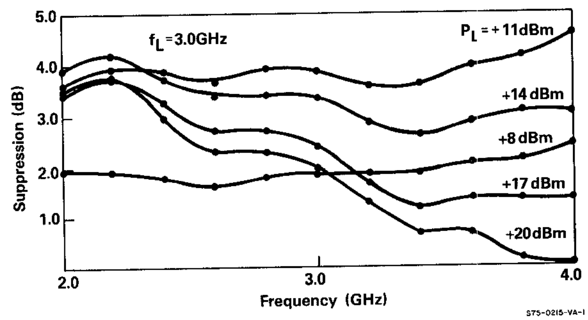


Figure 5 - Double anti-parallel pair limiter using Silicon diodes. f_L = 3.00 GHz, f_S = 2.95 GHz. C_j = .6 pf.

Figure 6 - Suppression characteristic as function of frequency and power level of GaAs device for large signal at 3.0 GHz.

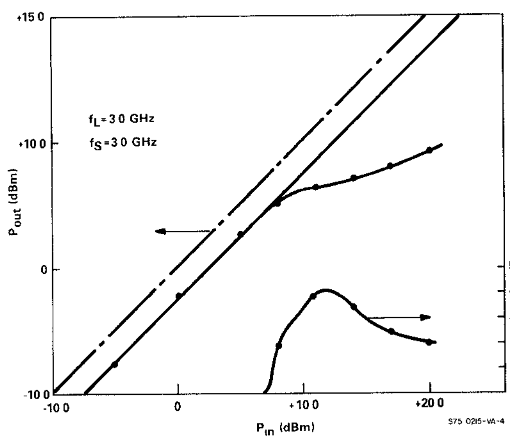


Figure 7 - Suppression and P_{out} as function of P_{in} at 3.0 GHz.